Priyanka C

Application Engineer | VLSI Design

Priyanka C holds an M. Tech degree in VLSI and Embedded Systems. Focused on developing practical solutions in both Digital and Analog domains. Has a proven track record in FPGA implementation and is gaining expertise in VLSI applications. Currently contributing to product development and technical solutions. Has expertise in training and mentoring engineering students and graduates in **VLSI SoC Design** for over 600 hours.

Academic interests span **Analog Circuit Design, RTL Verification, FinFET technologies, FPGA Development, Emulation and Prototyping, RISC-V Architecture, and 6G Communication, Low-Power and Mixed-Signal Design techniques.**

Proficient in **FPGA design using Verilog and VHDL**, Hardware Verification languages like **System Verilog and UVM**, and FPGA Implementation and Simulation tools like **ModelSim, Vivado and Quartus**. Skilled in industry-standard EDA tools such as **Synopsys, Cadence,** enabling her to efficiently manage design, simulation, verification, and prototyping tasks.

Worked as a Technical Support Executive at IBM, building strong troubleshooting, communication and client support skills. Also worked as an HR/Admin Executive at Jainco Industry Chemicals, strengthening organizational and coordination capabilities.

Published two conference papers in VLSI focusing on processor communication architectures and Analog circuit design optimization. Actively engages in workshops and technical training, consistently updating her knowledge through online courses and certifications. Passionate about public policy and national development, with active pursuit of the **UPSC Civil Services Examination** alongside her technical career.

Education:

- **M. Tech in VLSI & Embedded Systems**
- **B.E. in Electronics and Communication Engineering**

Professional Experience:
Total Years of Experience: 4 Years

- Application Engineer – RSA
- Technical Support Executive – IBM
- HR/Admin Executive – Jainco Industry Chemicals

Research Interests:

- VLSI SoC Design
- Analog & Mixed-Signal Circuit Design
- RTL Verification and Functional Testing
- FPGA Development, Prototyping and Emulation Techniques
- FinFET Device Technologies
- RISC-V Architecture
- 6G Technology

Technical Skills:

- ASIC Design Flow with Lint, CDC, STA
- RTL Design and Verification (Verilog, VHDL, SystemVerilog, UVM)
- TCL Scripting
- Analog Circuit Design and Analog Layout Design
- FPGA Design & Implementation (Xilinx Vivado, Intel Quartus)
- Block Level Prototyping and Debugging
- Design and Verification Tools (Cadence, Synopsys, ModelSim)
- RISC-V Architecture
- Programming Languages: C, C++, Python

Publications:

- RISC V Steel Processor Implementation for Communication between Two Chips using AXI Lite, published in Grenze International Journal of Engineering and Technology, June 2025

- Comparative Analysis of Multiple Input Bulk-Driven Operational Transconductance Amplifier in 0.18µm CMOS, published in Grenze International Journal of Engineering and Technology, June 2025

Certifications & Workshops:

- Participated in multiple workshops on ASIC Design, FPGA Design and RTL Verification.
    - ASIC Design Flow Workshop using Synopsys tools by NanoChip Solutions
    - RISC V Comprehensive Course by Aarfive Designs Pvt Ltd (4 Months)
    - RTL Verification Using System Verilog by Pro-V Logic
- Online certifications:
    - Principles of Modern CDMA/MIMO/OFDM Wireless Communications from NPTEL, 2025
    - VLSI Design Flow: RTL to GDS from NPTEL, 2024
    - Verilog HDL Fundamentals for Digital Design and Verification from Udemy, 2024
    - SystemVerilog for Verification from Udemy, 2024
    - Universal Verification Methodology (UVM) from Udemy, 2025
    - Synthesis-STA-Physical Design (PD) – Cadence & Synopsys Tool flow from Udemy, 2025
    - The Complete Course of Static Timing Analysis (STA) from Udemy, 2025