Darshan M R
Application Engineer | VLSI Design

Darshan M R serves as an Application Engineer at Ramaiah Skill Academy (RSA), bringing a strong background in VLSI design and Embedded Systems. He earned his Bachelor of Engineering in Electronics and Communication from the Cambridge Institute of Technology. Darshan has shown proven capability in both digital and analog sectors, with practical experience in FPGA implementation, RTL development, and hardware prototyping.

His academic interests **span Analog Circuit Design, RTL Design, RTL Verification, RTL Synthesis, FinFET technologies, FPGA Development, Emulation and Prototyping, RISC-V Architecture, SoC Design**, continually enhancing her skills in these domains

At RSA, he plays a key role in product development and technical service delivery, contributing meaningfully to VLSI-centric assignments. He is adept with **Verilog and** Hardware verification languages like **SystemVerilog and UVM**, and well-versed in using EDA platforms including **Synopsys, Cadence,** along with simulation& FPGA Implementation tools like **ModelSim ,Vivado and Quartus**,.

He continually sharpens his knowledge through professional workshops, hands-on training programs, and recognized online certifications in advanced VLSI, ASIC methodologies, and FPGA workflows.

Academic Qualification:

- Bachelor of Engineering in Electronics and Communication

Research Interest:

- System-on-Chip (SoC) Design
- Analog and Mixed-Signal Circuit Design
- RTL Verification & Functional Analysis
- FPGA Architecture, Prototyping & Emulation
- FinFET Technology
- RISC-V Processor Architecture

Technical Expertise:

- RISC-V Core Implementation
- RTL Design & Verification : Verilog, SystemVerilog, UVM
- TCL Scripting
- Lint, CDC, RDC, STA
- Physical Design in ASIC
- FPGA Architecture: Xilinx Vivado, Intel Quartus
- Design & Simulation Tools: Cadence, Synopsys, ModelSim
- Block-Level Prototyping and Debugging Techniques
- Programming languages: C, C++ , Python

Training:

- RISC-V Comprehensive Course by Aarfive Designs Pvt Ltd (4 Months)
- ASIC Design flow using synopsys by CCCIR (6 Months)

Certifications & Technical Events:

- Attended hands-on workshops on:
    - FPGA Architecture and Design
    - RTL Verification with System Verilog by Pro-V Logic
    - ASIC Design Lifecycle using Synopsys Tools by Nanochip Solutions
    - Arduino-Based Embedded Systems by Adhya Foundation
- Acquired certifications in:
    - Python Programming (Udemy, 2024)
    - Fundamentals of RISC-V ISA
- Held position as Co-Chair, Program Committee, IEEE Student Branch at Cambridge Institute of Technology
- Honoured with Best Paper Award for Technical Relevance at National Conference conducted in Cambridge Institute of Technology, Bangalore